International Workshop on **E**arly **R**eliability **M**odeling for **A**ging and **V**ariability in **S**ilicon **S**ystems

Co-Located with DATE - Dresden, Germany

Morning

Welcome and Opening		
8:30-8:40	Opening Remarks	Adrian Evans *IROC*
8:40-8:50	Clereco Project Overview	Stefano Di Carlo *Politecnico di Torino*
8:50-9:00	MoRV Project Overview	Domenik Helms *OFFIS*
Session I – Invited Talks Chair : Dimitris Gizopoulos – *University of Athens*		
9:00-9:45	The Resilience Wall: Cross-Layer Solutions	Subhasish Mitra *Stanford University*
9:45:10:30	Reliability Challenges for Large ASICs	Yongsheng Sun, *HiSilicon*
Session II – Poster Session Moderator : Domenik Helms - *OFFIS*		
10:30-10:45	Poster Introduction	
10:45-11:00	Poster Presentations and Coffee Break	
Session III – Tool Demos Moderator : Praveen Raghavan		
11:00-11:15	Tool Demos	
Session IV – Invited Talks Chair : Alberto Bosio - *LIRMM*		
11:15-12:00	Reliability and Safety Challenged for Automotive Devices	Wu-Tung Cheng, *Mentor Graphics*
12:00-13:00	Lunch	

Afternoon

Session V - Invited Talks Chair : Praveen Raghavan - *IMEC*		
13:00-13:40	Accuracy versus Breadth in Cross Layer Solutions	Rob Aitken *ARM*
Session VI - Embedded Tutorials Chair : Roland Jancke - *Fraunhofer*		
13:40-14:25	Reliability and Variability in CMOS Devices	Ben Kaczer *IMEC*
14:25-15:10	Aging Models for Analog Circuit Level Simulations	Peter Rotter *Infineon*
15:10-15:30	Poster Presentations and Coffee Break	
15:30-16:15	Aging on RT Level – Analysis and Monitoring	Ulf Schlichtman *Technical University Munich*
Session VII – Panel Session Moderator : Stefano Di Carlo – *Politecnico di Torino*		
16:15-17:00	Panel Session	*Ronald Newhard- IBM* *Riccardo Mariani –Yogitech* *Tiberiu Seceleanu - ABB* *Other panelists to be announced*
Wrap Up		
17:00-17:10	Closing Remarks	*Dimitris Gizopoulos* University of Athens

Poster Presentations

Title	*Authors*
Design–Reliability Flow and Advanced Models Address IC-Reliability Issues	Mohamed Selim, Eric Jeandeau and Cyril Descleves
Cross-Layer Approaches for an Aging-Aware Design Space Exploration for Microprocessors	Fabian Oboril and Mehdi Tahoori
NBTI Lifetime Evaluation and Extension in Instruction Caches	Shengyu Duan, Basel Halak, Rick Wong and Mark Zwolinski
Approximating Standard Cell Delay Distributions by Reformulating the Most Probable Failure Point	Dimitrios Rodopoulos, Philippe Roussel, Francky Catthoor, Yiannakis Sazeides and Dimitrios Soudris
Reliability-aware design method for CMOS circuits	Theodor Hillebrand, Nico Hellwege, Steffen Paul and Dagmar Peters-Drolshagen
Multi-Path Ageing Sensor for Cost-efficient Delay-Fault Prediction	Gaole Sai, Basel Halak, Rick Wong and Mark Zwolinski
Early Failure Prediction by Using in-situ monitors: Implementation and Application Results	Benhassain Ahmed
Ageing Impact on a High Speed Voltage Comparator with Hysteresis	Illani Mohd Nawi, Basel Halak and Mark Zwolinski
Overview of Health Monitoring Techniques for Reliability	Abhijit Deb, Bart Vermeulen and Luc van Dijk
Static Aging Analysis Using 3-Dimensional Delay Library	Haider Abbas, Mark Zwolinski and Basel Halak
LPVM: Low-Power Variation-Mitigant Adder Architecture Using Carry Expedition	Alireza Namazi and Meisam Abdollahi
Workload Impact on BTI HCI Induced Aging of Digital Circuits: A System Level Analysis	Ajith Sivadasan