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DATE 2016 – Early Reliability Modeling for Aging and Variability in Silicon System (ERMAVSS Workshop)

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Background for the Workshop

With the proliferation of integrated circuits implemented in the most advanced process technologies, there is a growing need to jointly analyze the effect of multiple sources of failures including variability and aging and to understand, early in the design cycle, their impact on system reliability. Today, conservative margins are required to ensure that devices operate correctly over their full lifetime, despite the impact of aging effects (BTI, HCI) and failure mechanisms such as EM. New methodologies for improved cross-layer modeling and mitigation, if planned early in the design of a product, have the potential to remove unnecessary conservatism, reduce power and cost and improve yield. This workshop is focused on sharing new research on techniques and methodologies for modeling the effects of failures due to transistor aging, variability and other mechanisms all the way from the cell level to system level. New approaches to perform early estimations of system reliability are much needed to enabling reliable, optimized and low-power designs.

The Specific topic for the panel session is :

Permanent failures (EM, DB), Aging Failures (HCI, xBTI) and intermittent failures (radiation effects) are all serious threats to the reliable operation of integrated circuits. Which class of failures poses the most serious threat to today's large integrated circuits when they are deployed in the field? Pick one and defend your position. Please bring as much quantitative data as possible to defend your position.

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Chip Lifetime Reliability

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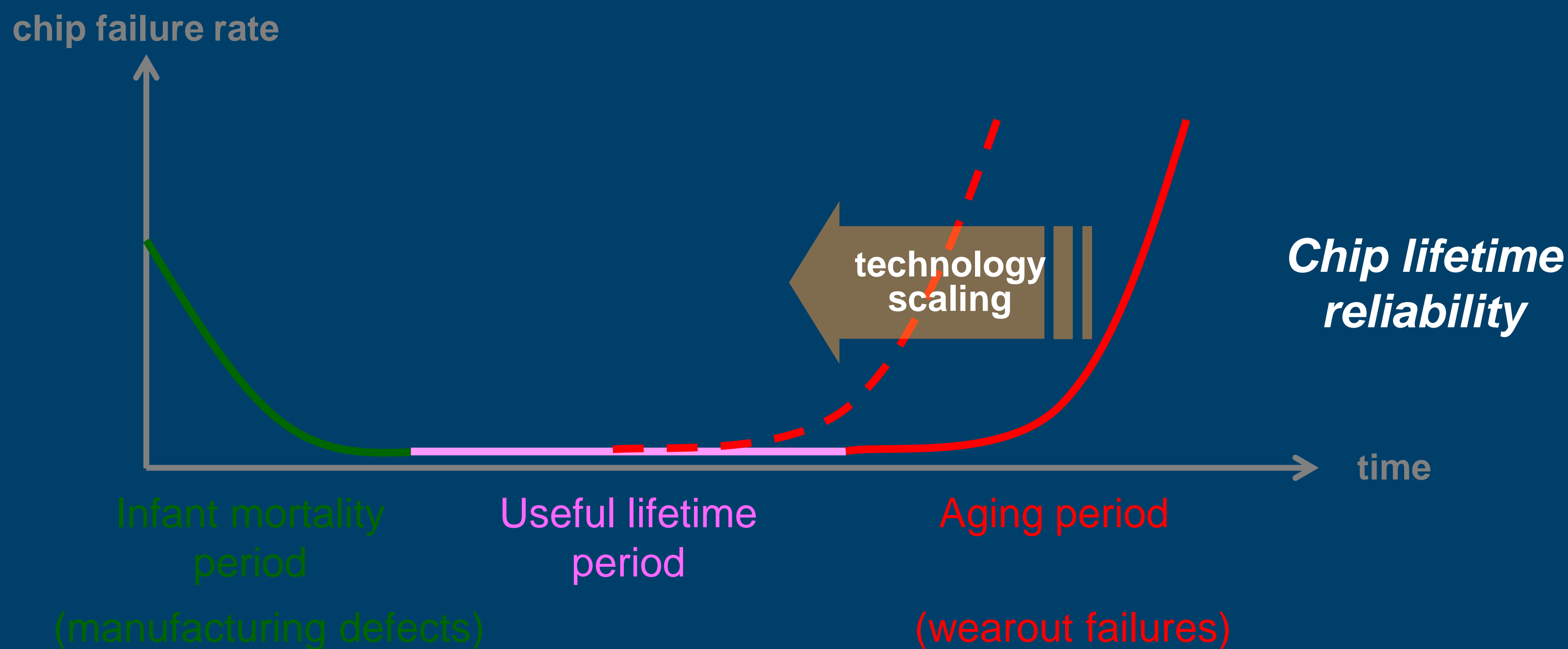

Technology scaling

- **Reduced gate oxide thickness and interconnect feature size**
- **Non-ideal supply voltage scaling**
- **Higher power densities**
- **Higher total number of transistors**

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Future Reliability Challenges from an EOL Perspective

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Ranking	Reliability Mechanism	Factors Impacting Possible EOL Failures
1	BTI – Bias Temperature Instability	1. BTI is Very Duty Cycle Dependent 2. Delta in NBTI vs PBTI → Technology Dependent (Beta Ratio) - Impact to Beta Ratio / Timing 3. Increasing w/ Replacement Metal Gate / FinFET 4. Static Registers & "Stagnant" Array Cells Worst Case 5. Easy to Accelerate with Stress & BIST, But Difficult to Model Actual Application (BIST vs Functional). 6. Nominal Modeling Capability w/ RelXpert.
2.	TDDB (Low K)	1. Targeting Larger Vias to Improve Yield (Via-> Line Space) 2. Critical Dimension (CD), Overlay, and Line Edge Roughness all Make TDDB more difficult. 3. Along with BTI, Limits Vmax for Given Technology Node
3.	Electro-migration	1. Localized Exposure due to Self Heating & Circuit Hot Spots 2. Lithography Non-Uniformities Also Difficult to Model 3. Very Difficult to Accelerate with HTOL Stress
4.	HCI	1. Worst Case at High Temp 2. Device Level Self-Heating → Hot Buffers, Difficult to Model 3. Inherently Higher HCI w/ Fin Structure 4. Ability to Extend Rel-Xpert Models to 10nm & 7nm
5.	Soft Error Rate (SER)	1. Hot Source Testing to Validate Models 2. Circuit Mitigation using Stacked Devices 3. Fault Injection Models

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Future Reliability Challenges from an EOL Perspective

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❑ General Observations about Intrinsic / EOL Reliability Challenges:

- Need Development of Combined Device Degradation Model → BTI & HCI
  - Model Overall Performance Degradation
  - Include Capability for BTI/HCI Tradeoff Options

- Reliability Models Required Early in the Technology Cycle Prior to Base Technology Qualification
  - Facilitates Design for Reliability Early in the Design Cycle

- Statistical Process Variability Is Eroding EOL Margins for Most Intrinsic Mechanisms
  - Line Edge Roughness as function of Critical Dimension
  - Overlay Variance with Multiple Exposure Levels
  - Device VT Variation vs Layout and w/in chip → Eroding EOL Margins

- Increasing Rate of Material Changes by Technology Generation
  - New Material Requires Reliability Evaluation to Understand Implication to Intrinsic Mechanisms
  - Limited Baseline of Intrinsic Reliability Characteristics on new Material
  - Increases Difficulty to Provide Early Models to Designers

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Future Reliability Challenges from an EOL Perspective

Mechanism	Random Logic	Array (SRAMs & Register Files	Analog Circuits PLL / VCO	I/O Circuits	High Speed Serial Interfaces (PCIE..)
1. BTI	High - Critical Paths - Beta Ratio - Latch Stability	High - Signal Margin Sense Amp - Cell Stability - Write-ability	High - Function Depends on Min Device Shift	Med - Potential Impact to Data Eye	High - High Speed Interfaces More Susceptible to Data Eye Shift
2. TDDB	High - Tightest GRs in Core Logic	Med - Dense Cell GRs	Med-Low - Analog GRs More Relaxed	High - Higher Supply Voltages	Med - High Speed Drivers
3. Electro-migration	High - Highest Juse in Core - Hot Spots	Low - Lower Juse	Low - Lower Juse	Med-High - High Current Drivers	Med - High Speed Drivers
4. HCI	Med - Depends on Duty Cycle	Low - Arrays < Peak Core Temp	Low - Relaxed Analog Dev.	Med - High Current Drivers	Med - High Speed Drivers
5. Soft Error	Med-High - Latch Stability	Low - ECC + Parity	Med - Low Critical Area	Low - High Current Drivers Not Susceptible	Low - High Current Drivers Not Susceptible

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Wearout Failure Mechanisms

- Electromigration (EM)
- Bias Temperature Instability (BTI)
- Time Dependent Dielectric Breakdown (TDDB)
- Hot Carrier Injection (HCI)
- etc.

- *Strong temperature dependence in many of these failure modes!*
- *Of increasing concern in post-22nm nodes*

Key observations

- **Failure mechanisms affect only certain types of on-chip devices**
- **The wearout of devices progresses only if the stress conditions of failure mechanisms are applied**
- **The wearout of devices may be reversible**

J. Shin et al. DSN 2007, ISCA 2008

Architecture-level lifetime reliability modeling framework

(supercedes earlier RAMP model: 2005)

Proactive wearout recovery approach

(wear leveling)

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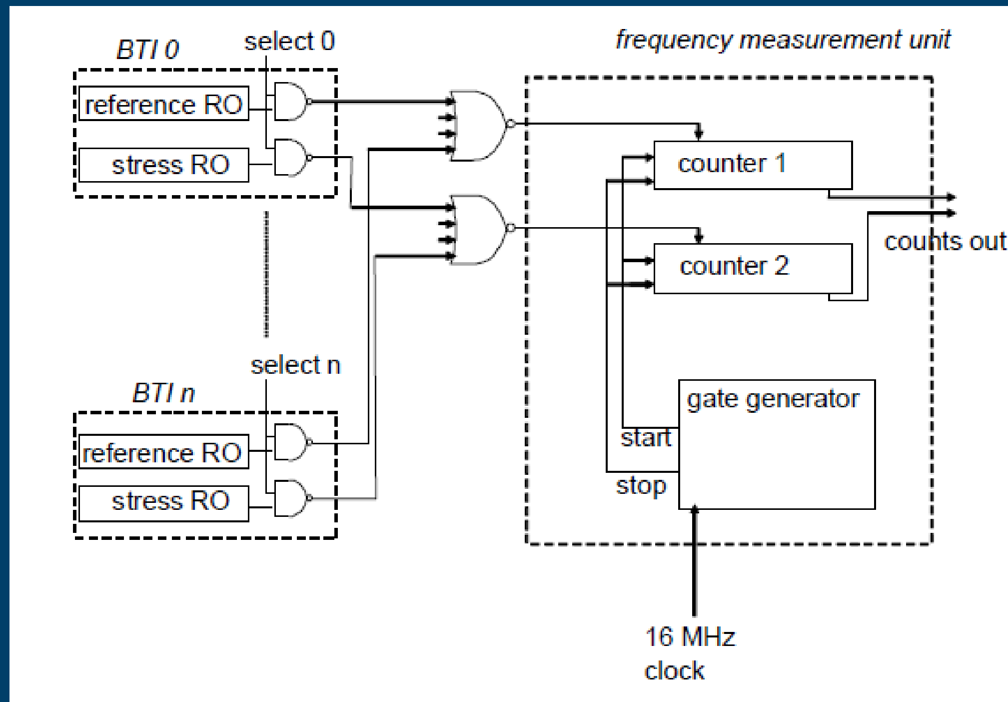
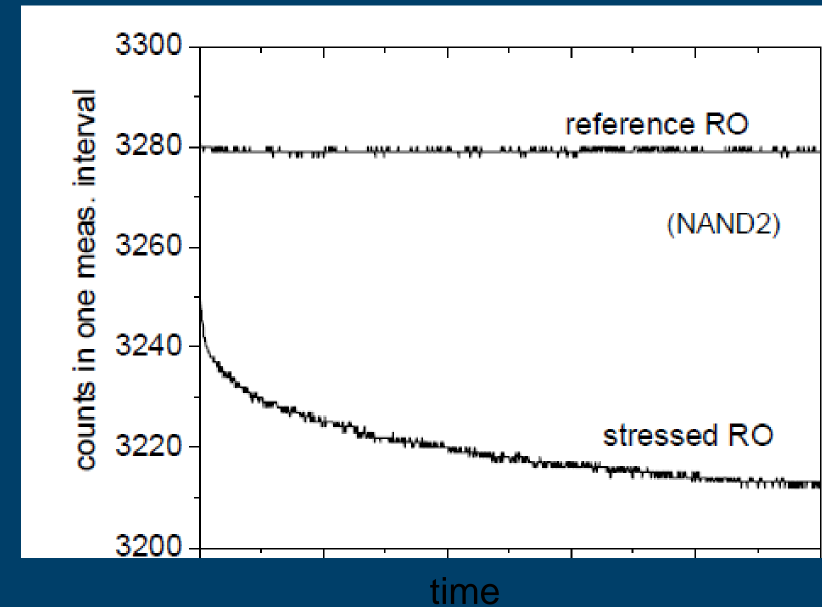
Transistor BTI / HCI Degradation Product Monitor





- Several ring oscillator pairs on each chip
- A pair consists of a stressed RO (running all the time) and a reference RO (running only briefly one a week, when tested)
- The stressed RO slows down due to BTI, while the reference RO does not
- The ratio provides a measure for transistor degradation

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Transistor BTI / HCI Degradation vs Targets

- Long term field data are more accurate than lab data
- Transistor degradation margin (BTI) was cut in half directly resulting in higher performance

Transistor BTI / HCI Degradation vs Targets

Old Target

New Target

System A

System B

RO Frequency Degradation [%]

0

365

730

Time [days]

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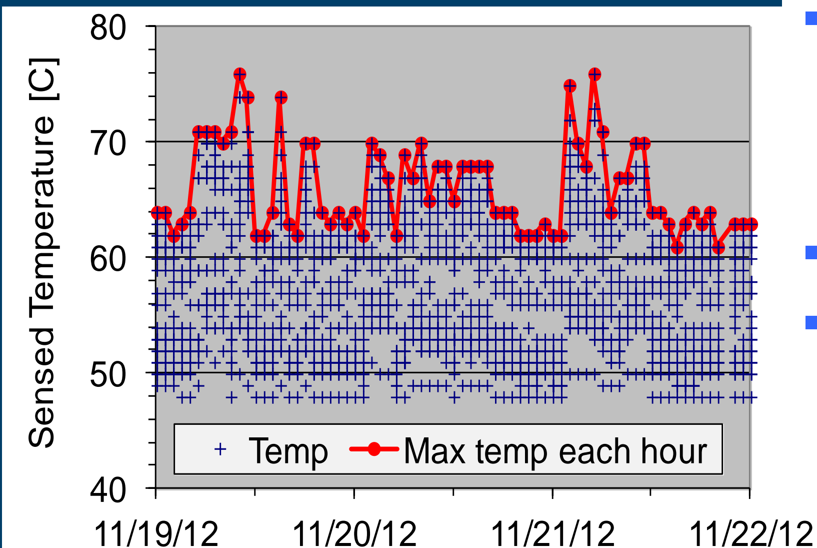
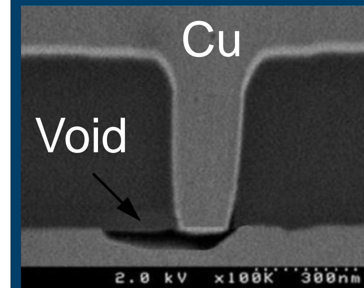
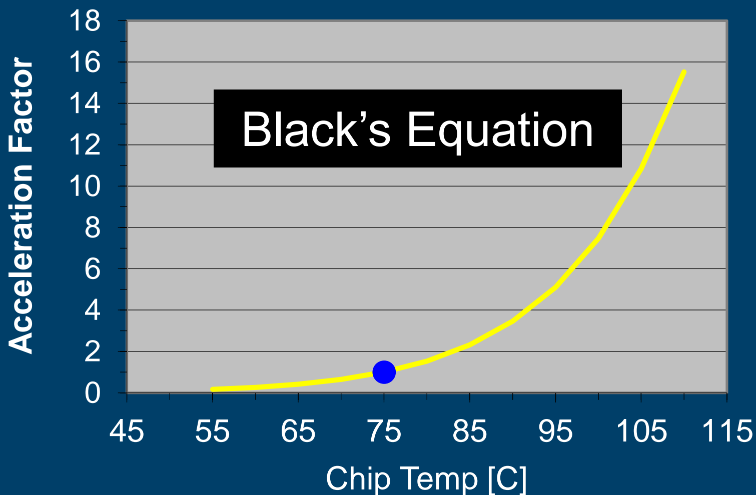
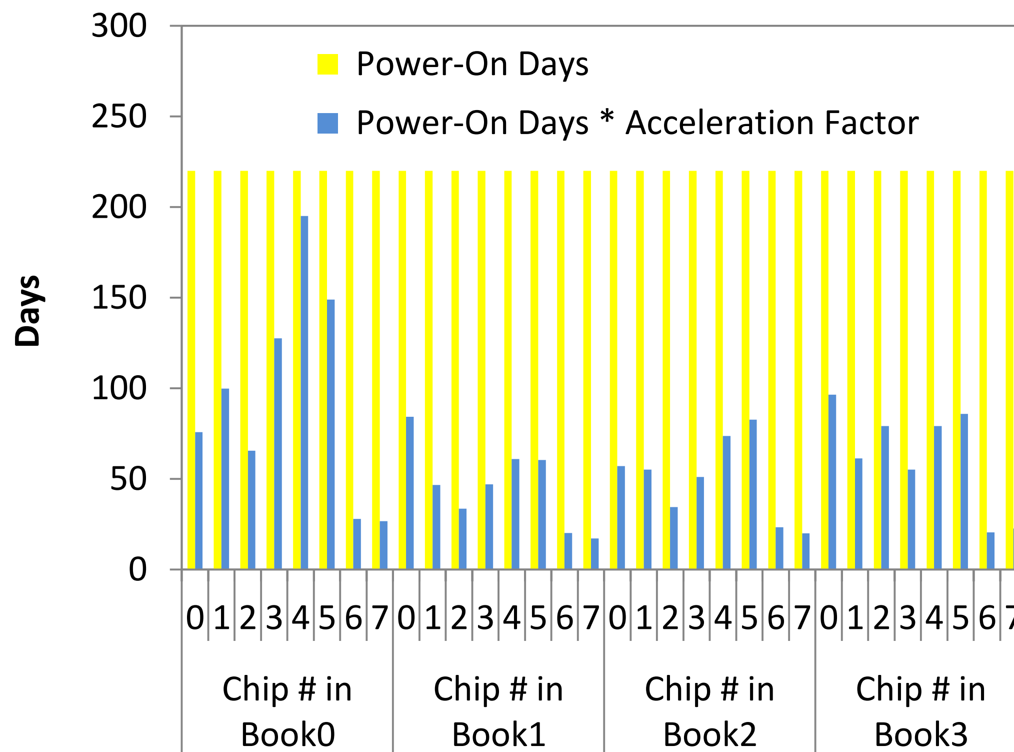
Remote Electromigration Monitor



- Electromigration: Metal moves faster for hotter chips, slower for cooler chips, voids can form
- Chips are actively monitored
- Pat.Appl. US 20140278247 A1







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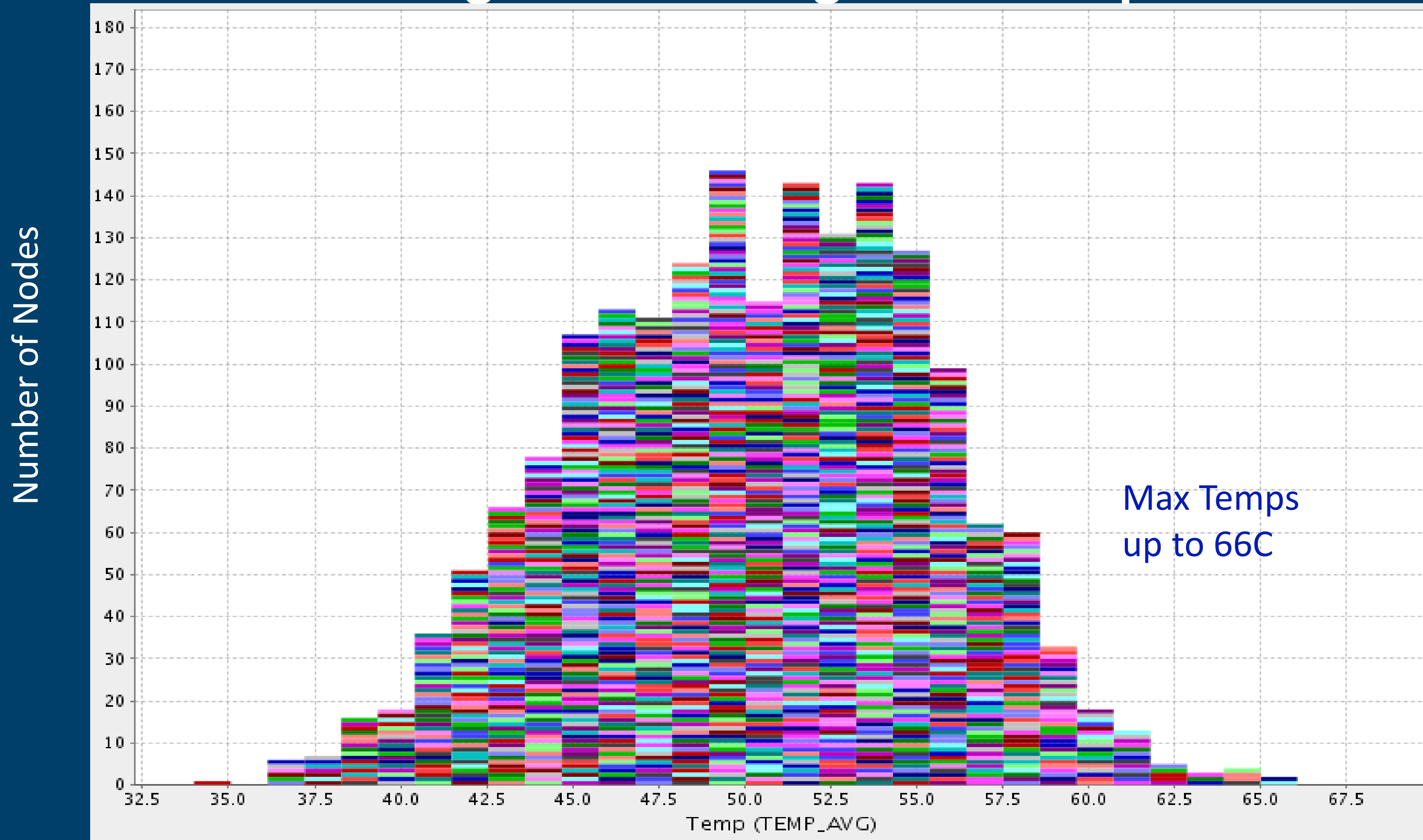
Power/performance vs targets



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Future Reliability Challenges – Strategic Risk Mitigation Elements

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- **Design for Manufacturability & Reliability**
  - DTCO – Design Technology Co-Optimization
  - Early Reliability Models Embedded in Groundrules & Simulation Tools
- **Rigorous Technology Qualification Methodologies**
  - Stress of Representative "Product Like" Structures
  - DC & AC Stress Techniques Based on Mechanisms
  - Utilize Product (vs Testsites) Early Within the Technology Qualification Cycle
  - Refinement of Reliability Models by Technology Node Based on Qualification Learning
- **Aggressive Physical & Electrical Screens Based on Qualification Learning**
  - Maverick Limits to Protect Intrinsic Reliability Mechanisms
  - Implementation of High Corner AC Screens to Capture Subtle T0 Fails
  - Continuous Learning / Adjustment Based on On-going Reliability Monitoring (ORM)
- **System RAS optimization to detect / auto-correct Faults where-ever possible**
  - Parity Checkers / Error Correction
  - In-Situ Repair Capability

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Future Reliability Challenges – Data Analytics

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- **Analytics Provides Tools to Improve Reliability and Decrease Risk**
  - Qualification Data vs In-Line Fab Data
  - Wafer Final Test Yield Data w/ High Voltage Screen
  - Manufacturing Burn-in Fallout Correlation to Wafer Test & Fab Data
  - System Performance & Environmental Data
  - Integration of Above Data into Common Platform to Enable Continuous Learning

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Back-up

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Future Reliability Challenges from an EOL Perspective

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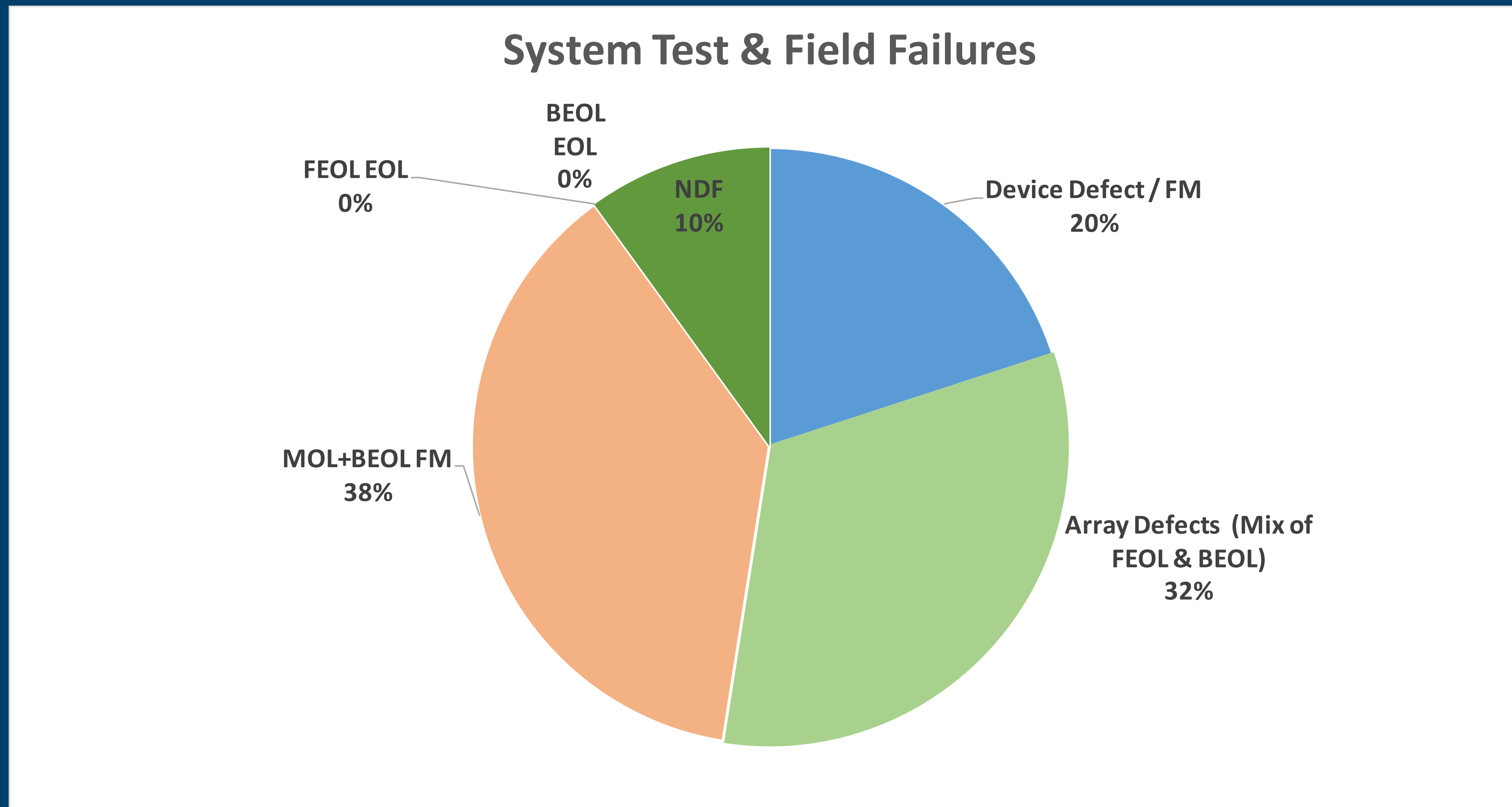
- Current System Test & Field Data → No Indication of EOL Type Wear out Failure Mechanisms



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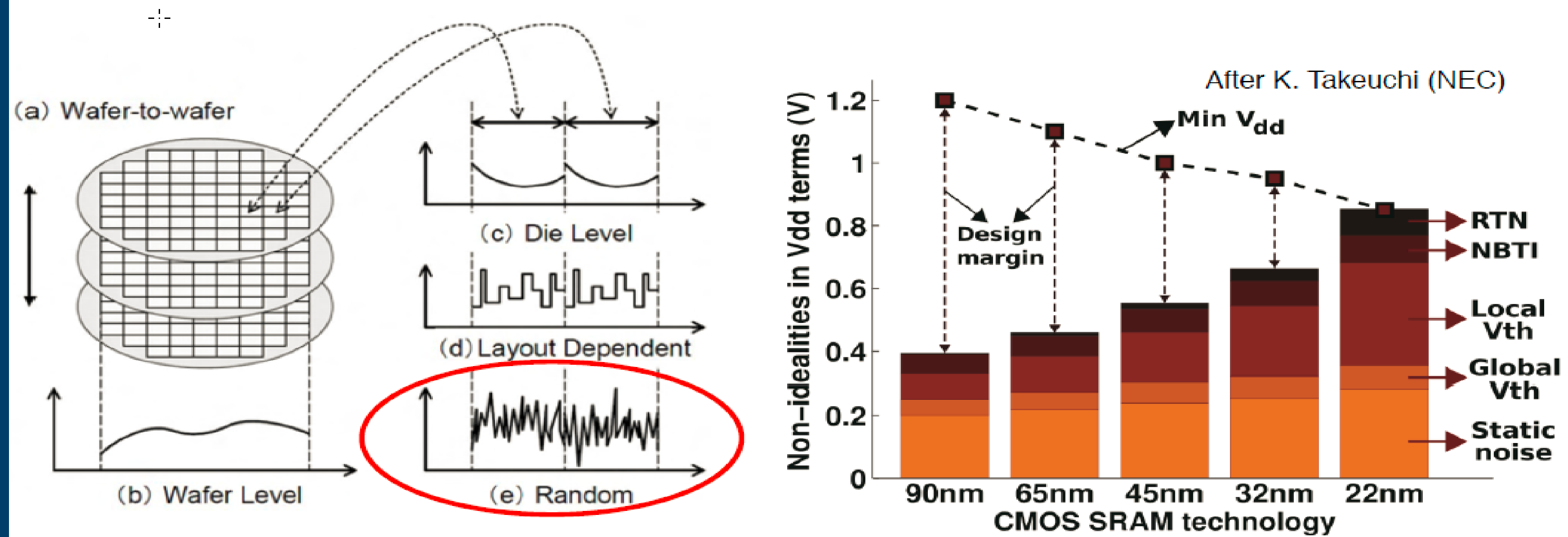
Statistical variability is one of the major challenges associated with scaling



Variability results in higher parametric yield loss

Source: Design/Technology Co-Optimization (DTCO) in the Presence of Acute Variability. A. Asenov, E. A. Towie

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Long-term data for BTI degradation in 32nm IBM microprocessor using HKMG technology

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***Abstract*—This paper describes the measured long-term BTI field data from IBM zEnterprise EC12 systems in 32nm High-k/Metal Gate (HKMG) technology using a built-in monitor which is capable of separating the PBTI and the NBTI effects. The BTI monitor is accompanied by a digital thermal sensor in close proximity to correlate the BTI degradation with temperature. Comparable PBTI and NBTI degradation in use condition were observed. Compared with previous z196 microprocessor with 45nm SiON CMOS technology, the new 32nm zEC12 showed more than 2X less BTI degradation. This is attributed to HKMG technology optimization and lower chip voltages.**

Keywords- BTI, NBTI, PBTI, monitor.

I. Introduction

With the advent of high-dielectric metal gate (HKMG) stack in CMOS technologies of 32nm and beyond to counter the gate

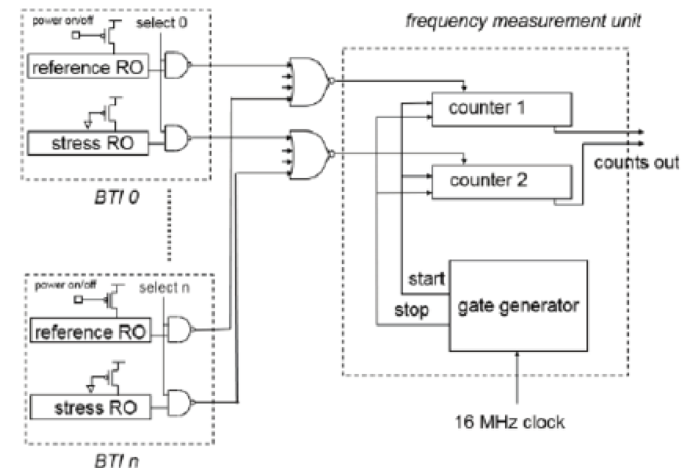

Fig. 1: The Block diagram of the implementation of BTI monitors in an IBM z microprocessor [9].

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