RELIABILITY AND VARIABILITY IN CMOS DEVICES

PRESENT STATUS OF CIRCUIT SIMULATIONS

Time-zero + Reliability+Projection = Combined effect

- nFETs 11G
  - $V_{ds} = 50\text{mV}$
  - High $V_{\text{THEX}} > +5.4\sigma$
  - Mid $V_{\text{THEX}} \pm 3.7\sigma$
  - Low $V_{\text{THEX}} < -5.4\sigma$

- $T = 125^\circ\text{C}$
  - $V_{G,\text{stress}} = -2\text{ V}$
  - $V_{G,\text{relax}} = 0\text{ V}$

- Acceleraion for BTI, HCI, ...

- Mean $\Delta V_{th}$

- normal Distribution ($\sigma$)

- $V_{\text{THEX}}$ (V)

- $P$

- $0 \rightarrow$ operating time

- $0 \rightarrow$ operating time

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CIRCUIT SIMULATIONS WITH VAR/REL

RTN @ time-zero

BTI, HCl,… variability

Time-zero

Rel/Var+Projection

Combined effect
MOTIVATION

How to best describe and how to include time-dependent variability in circuit design
OUTLINE

Motivation

Time-dependent variability
  ▶ The short version: Gate-oxide Breakdown ($I_G$)
  ▶ The full scoop: BTI and RTN ($I_D$)
    ▶ Reliability from Defect-centric perspective
    ▶ Measuring and modeling single defect properties
    ▶ Distributions of single defect properties
    ▶ Multiple-defect statistics

Combining time-dependent and time-0 variabilities

Combined variability in circuits
APPEARANCE OF TIME-DEPENDENT VARIABILITY:
BREAKDOWN IN THIN GATE OXIDES WIDELY DISTRIBUTED

- Gate oxide breakdown (TDDB) statistical distribution is linked to number of traps in percolation path
- With scaled down dimensions the intrinsic spread on the reliability parameters (e.g. $t_{BD}$ or $Q_{BD}$) tends to increase (percolation model)

\[ F(t) = 1 - \exp \left[ -\left( \frac{t}{\eta} \right)^\beta \right] \]
CIRCUIT FAILURE DISTRIBUTION CAN BE PROJECTED FROM DISTRIBUTIONS OF SINGLE DEVICES

\[ V_{OSC} = 4.4 \text{ V} \]

\[ V_{INP} = 0 \text{ V} \]

\[ F_{osc}(t) = 1 - \left[ 1 - F_n(t) \right]^{N_n} \times \left[ 1 - F_p(t) \right]^{N_p} \]

\( t_{BD} \) distribution of individual n- and pFETs scales perfectly to ring oscillator time-to-1st-BD distribution

Kaczer et al., TED 49, p. 500 (2002); Microel. Reliab., 2002

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IN ADDITION, DISTRIBUTION OF BD PROPERTIES

• Distribution BD locations

• Distribution BD magnitudes

Alam et al., TED 2002
DISTRIBUTIONS OF BD IMPACT ON CIRCUIT PARAMS

• Example: Impact on RO frequency, power consumption

Kaczer et al., TED 49, p. 500 (2002); Microel. Reliab., 2002
http://www.youtube.com/watch?v=BdFydfGAx3w

• Other examples:

Wang et al., IEEE MTDT 2006

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Combined variability in circuits
In deeply-downscaled technologies, only a handful of random defects will be present in each device.

Number of charged defects will be increasing with operating time → **time-dependent variability** in addition to time-0 variability.
INDIVIDUAL DEFECTS RESULT IN TIME-DEPENDENT VARIABILITY

- Individual stochastically-behaving **charged** defects will affect FET channel current
- Individual defects have considerable *relative* impact on deeply-scaled devices
- These **time-dependent variations** require adaptations in circuit design to account for **time-dependent statistical distributions** of device parameters
IN GENERAL, EACH DEFECT CHARACTERIZED BY

• capture time $\tau_c$
• emission time $\tau_e$
• impact on device ($\Delta I_d$, $\Delta V_{th}$, $\Delta I_g$…)
• occupancy (0 or 1) at given time

(covers BTI, RTN, SILC, ... easily extensible to other mechanisms)

EACH DEVICE CHARACTERIZED BY

• number of defects $N_T$ with above properties

Example: defects in 3 different devices

Depend on
• spatial position
• energy position
• lattice relax. energy
• ...

Kaczer et al., IRPS 2011
DEFECT-CENTRIC VIEW OF RELIABILITY

From individual defect properties to logic gate level and beyond

Understanding of degradation mechanisms at individual defect level is essential for simulations of time-dependent variability in circuits
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Combined variability in circuits
SIMPLE EXPERIMENTAL SETUP

$L \times W = 70 \times 90 \text{ nm}^2$

DC or AC stress

$V_G (V)$

$V_{STRESS}$

$t_{STRESS}$

$t_{H}$

$t_{L}$

$time (s)$

Source current $I_s (\mu A)$

$t_{RELAX}$

$t_{STRESS}$

$m.nSi$

Poly-Si

SiO(N)

$p^+$

$p^+$

$n-Si$

-0.1V

$\Delta I_s$ to $\Delta V_{th}$

Initial $I_s-V_G$ used to convert

$\cdot$ M. Toledano et al., IRPS 2011

$\cdot$ B. Kaczer et al., IRPS 2005 & 2008

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WHAT WE CAN MEASURE

- Emission time of a **single** trap
- (Average) **single** trap occupancy
- Capture time of a **single** trap
- Impact of a **single** trap on FET chars for multiple traps

As a function of $V$, $T$, AC duty

Full IV after charging of a **single** trap

TDDS spectrum

Grasser et al., IRPS 2010; Toledano et al., INFOS 2011; Franco et al., IRPS 2012
NON-RADIATIVE MULTIPHONON MODEL REPRODUCES VOLTAGE AND TEMPERATURE DEPENDENCES

2-component process

Relaxation MPE

Typical RTN window

\[ \tau_c(S), \tau_e(S), f_p(\cdot) \]

Data by H. Reisinger, Infineon
Grasser et al., IRPS 2009, 2010;
IEDM 2009, 2010;
PRB 2010

Schanovsky, Görs, and Grasser
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Coupling = \frac{kT}{q} \frac{\partial \ln \tau}{\partial V_G}

“slope” of \( \tau(V) \) plot

Rzepa et al., SISPAD 2015

Miki et al., IEDM 2012
... AND BTI (AND CAPTURE/EMISSION TIME MAPS IN LARGE DEVICES)

\[ \tau_e(s) \]

\[ -V_G (V) \]

\[ \tau_c(s) \]

\[ V_G^L = -0.35 \text{ V}, \quad V_G^H = -1.45 \text{ V} \]

Capture/Emission Time (CET) Map
INCORPORATION OF WORKLOAD DEPENDENCE INTO CIRCUIT SIMULATIONS

Defect properties

Workload

log(τ_c) vs log(τ_e)

CET-active map describes the distribution of the occupied traps after workload specific for each device.
$\Delta V_{TH}$'S DUE TO SINGLE TRAPPED CHARGES
~EXPONENTIALLY DISTRIBUTED

$\tau_e(V, T)$

$\tau_c(V, T)$

(size of bubble represents impact)

$f_1(\Delta V_{th}, \eta) = \frac{e^{\frac{-\Delta V_{th}}{\eta}}}{\eta}$

$\eta = 4.75$ mV

$t_{stress} = 1900$ s

$\eta (V) =$ expectation value = average shift per elementary charge
CAUSE: RANDOM DOPANT FLUCTUATIONS IN THE CHANNEL

Channel current non-uniform: flows via percolation paths

- Most traps influence channel current flow little
- A few traps influence channel current a lot
SCALING OF $\eta$

Average shift per $q$

$$\eta = \frac{B \eta}{WL}$$

Scales reciprocally with gate area

Scales with $t_{inv}$ and $N_A$ (via $x_d(V_B)$)

$A = (2H_{fin} + W)L$ (nm$^2$)

Scales with $t_{inv}$ and $N_A$ (via $x_d(V_B)$)

J. Franco et al., IRPS 2012 & 2013
DIFFERENT TECHNOLOGIES HAVE DIFFERENT SUSCEPTIBILITY TO TRAPS

Single trap $\Delta V_{th}$ distribution in presence of trapped charges

$N_T = 5 \times 10^{11} \text{ cm}^{-2}$

$N_T = 1 \times 10^{12} \text{ cm}^{-2}$

$W_{Bulk/FDSOI} = W_{eff. \text{FinFET.}} = 60 \text{nm}$

RDD, LER, MGG

Uniform

1-CDF

Threshold shift $\Delta V_T$ (mV)

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BTI STATISTICS FULLY DESCRIBED BY DEFECT-CENTRIC DISTRIBUTION

\[ H_{\eta,N_T}(\Delta V_{th}) = \sum_{n=0}^{\infty} e^{-N_T} \frac{N_T^n}{n!} \left[1 - \frac{n}{n!} \Gamma(n, \Delta V_{th}/\eta)\right] \]

- Known statistics $\rightarrow$ all moments can be derived
- Corollary: reporting “best” devices a delusion [Franco et al., IEDM 2014]

\[ \eta = \langle \text{single defect impact} \rangle \]
\[ N_T(t) = \langle \# \text{ of active defects per device} \rangle \]
IMPORTANCE OF CORRECT STATISTICS FOR $V_{\text{MIN}}$ PREDICTION

II. BTI VARIABILITY FRAMEWORKS: A COMPARISON

Both Rauch [1, 3] and Kaczer et al. [4] have published frameworks that aim to comprehend BTI variability in ultra-scaled MOSFETs through the use of Dispensive Skellam (DS) and Exponential-Poisson (EP) distribution statistics respectively. The corresponding cumulative distribution

Figure 11. Time-zero and post-aging $VT$ distributions on 22nm data-sets of (top) ~ 3,100 transistors and (bottom) ~ 92,000 transistors are studied to understand potential deviations from normality due to aging degradation.

Bias Temperature Instability Variation on SiON/Poly, HK/MG and Trigate Architectures

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C. Auth, K. Mistry, S. Natarajan, P. Packan, I. Post
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Components Research, Intel Corporation, Hillsboro, Oregon 97124, U.S.A.

Figure 14. Actual assessment of $V_{\text{MIN}}$ on a circuit block with over 20,000 repeated instances demonstrates the importance of using the correct statistical variation framework for BTI simulations.
APPLICATIONS OF DEFECT-CENTRIC DISTRIBUTION

- **Si BTI**

  - Si Channel Hot Carrier (CHC)

  - Stress time dependence

    - Stress time dependence

    - L. Procel et al., accepted EDL

- **SiGe BTI**

  - Tail of the distribution

  - Average

  - J. Franco et al., TED 2013

- **InGaAs finFET BTI**

  - J. Franco et al., IEDM 2014
MULTIMODAL TIME-DEPENDENT STATISTICS DERIVED

32 K FET array

NFETs: Bimodal distribution

\[ H_{\eta_1,\eta_2,N_{T1},N_{T2}}(\Delta V_{th}) = \sum_{n_1=0}^{\infty} \sum_{n_2=0}^{\infty} \frac{e^{-N_{T1}}}{n_1!} \frac{e^{-N_{T2}}}{n_2!} F_{n_1,n_2,\eta_1,\eta_2}(\Delta V_{th}) \]

P. Weckx et al., IRPS 2015
see also A. Subirats et al., TED 2015

Note: circuits are also designed to measure time-dep’t var!
CONVERTING BETWEEN MINDSETS

Time-dependent variability

Technology
Avrg. number of defects $N_T$
Average impact per defect $\eta$

$N_T(t) = 2\frac{\langle \Delta V_{th}(t) \rangle^2}{\sigma_{\Delta V_{th}}^2}$

$\eta = \frac{\sigma_{\Delta V_{th}}^2}{2\langle \Delta V_{th}(t) \rangle}$

Design
Average shift $\langle \Delta V_{th} \rangle$
Variability $\sigma_{\Delta V_{th}}$

$\langle \Delta V_{th}(t) \rangle = \eta N_T(t)$

$\sigma_{\Delta V_{th}}^2(t) = 2\eta^2 N_T(t)$

$\sigma_{\Delta V_{th}}^2(t) = 2\eta \langle \Delta V_{th}(t) \rangle$

• $\eta$ is a measure of time-dependent (dynamic) variability due to RTN, BTI, HCl, etc.
• $\eta$ can be extracted from the $\Delta V_{th}$ distribution
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Combined variability in circuits
### TIME-0 & TIME-DEP’T VAR ARRAY DESIGNED

**M. Simicic et al., IIRW 2015**

**V. Putcha et al., IIRW 2015**

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**Transmission gates, level shifters, shift registers**

**pMOS 150x100**

**pMOS 30x3x100**

**pMOS 90x100**

**pMOS 30x100**

**pMOS 30x200**

**pMOS 30x300**

**nMOS 30x300**

**nMOS 30x200**

**nMOS 30x100**

**nMOS 90x100**

**nMOS 30x3x100**

**nMOS 150x100**

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**54 432 DUTS**

**1 000 DUTS**

**1 400 DUTS**

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TIME ZERO VARIABILITY FROM ARRAY

PMOS devices with minimum length have a higher variance:

- Explained by the nonlinear interplay of the LER with the short channel effect in minimum length devices

\[ \sigma_{V_{TH0}}^2 = \frac{A_{vth}^2}{WL} \]

[D. Reid, A. Asenov, TED, vol. 57, no. 11, 2010.]

M. Simicic et al., IIRW 2015
TIME-DEPENDENT VARIABILITY FROM ARRAY

\( t_{\text{stress}} = 1000 \text{s} \)
\( V_{\text{stress}} = -1.4 \text{ V} \)
\( V_{\text{relax}} = -0.55 \text{ V} \)
\( LW = 30 \times 100 \text{ nm}^2 \)

\[ \eta = \frac{B\eta}{WL} \]

\[ N_T = N_{ot} \cdot WL \]

Recall:
\[ \langle \Delta V_{th}(t) \rangle = \eta N_T(t) \]

\[ \sigma_{\Delta V_{th}}^2(t) = 2\eta \langle \Delta V_{th}(t) \rangle \]

M. Simicic et al., IRPS 2016
INITIAL AND TIME-DEPENDENT VARIABILITY

Technology characterized by initial (time-zero) and time-dependent variances

- pFET this array (40 nm foundry)
- nFET this array (40 nm foundry)
TIME-DEPENDENT VAR ADDS TO TIME-0 VARIABILITY

\[ V_{TH}(t) = V_{TH0} + \Delta V_{TH}(t) \]

Initial \( V_{TH0} \) variability

Time-dependent \( \Delta V_{TH} \) variability

\[ \sigma^2_{\Delta V_{TH}}(t) = 2\eta \left\langle \Delta V_{TH}(t) \right\rangle \quad \text{&} \quad \eta = \frac{B_{\eta}}{WL} \]

Total \( V_{th} \) distribution

\[ K(V_{TH}) = \int_0^\infty g_{V_{TH0},\sigma_{TH0}}(V_{TH} - V) H_{\eta,\Delta V_{TH}/\eta}(V) dV \]

Low \( V_{TH} \) (\( \sigma = 28 \text{mV} \))

Mid \( V_{TH} \) (\( \sigma = 3.7 \sigma \))

High \( V_{TH} \) (\( \sigma = 5.4 \sigma \))

LxW = 35x90 nm²

Kuhn et al., TED 2011

T. Mizutani et al., IEDM 2013

Kaczer et al., EDL 2015

T. M. Mizutani et al., IEDM 2013
OUTLINE

Motivation

Time-dependent variability

▸ The short version: Gate-oxide Breakdown ($I_G$)
▸ The full scoop: BTI and RTN ($I_D$)
  ▸ Reliability from Defect-centric perspective
  ▸ Measuring and modeling single defect properties
  ▸ Distributions of single defect properties
  ▸ Multiple-defect statistics

Combining time-dependent and time-0 variabilities

Combined variability in circuits
DIFFERENT WAYS TO INTRODUCE DEGRADATION INTO CIRCUIT SIMULATIONS

LEVEL 1
Constant stress → Mean degradation

LEVEL 2
Multi stress → Mean degradation

LEVEL 3
Multi stress → Mean degradation + variability

LEVEL 4
Multi stress → Variability + RTN

Complexity, accuracy

Constant stress → Mean degradation

Multi stress → Mean degradation

Multi stress → Mean degradation + variability

Multi stress → Variability + RTN

<ΔV_th>
FETs IN STANDARD CIRCUIT NETLIST INSTANTIATED WITH INDIVIDUAL TRAPS
THE CIRCUIT IS SOLVED WITH INDIVIDUAL DEFECT BIAS-TIME (I.E., WORKLOAD) DEPENDENCES
“ATOMISTIC” CIRCUIT SIMULATOR: ALLOWS TO FOLLOW INDIVIDUAL DEFECT EVENTS

Kaczer et al., IRPS 2011
DIFFERENT WAYS TO INTRODUCE DEGRADATION INTO CIRCUIT SIMULATIONS

**LEVEL 1**

Constant stress → Mean degradation

**LEVEL 2**

Multi stress → Mean degradation

**LEVEL 3**

Multi stress → Mean degradation + variability

**LEVEL 4**

Multi stress → Variability + RTN

Complexity, accuracy
IMPACT OF TIME-DEPENDENT VARIABILITY: EXAMPLES

Low-sigma designs: logic

High-sigma designs: memory

Product Binning
NON-MC PROPAGATION OF DISTRIBUTIONS TO OUTPUT PARAMETER VIA RESPONSE SURFACE

Projected total $V_{th}$ distributions

$$g(\xi) \int_{C_i} g(\xi) d\xi$$

SRAM SNM response surface

SRAM SNM response surface

Projections to $\pm 7\sigma$ possible!
THE DEFECT-CENTRIC PERSPECTIVE OF DEVICE AND CIRCUIT RELIABILITY—FROM INDIVIDUAL DEFECTS TO CIRCUITS

- Time-dependent variability needs to be considered in addition to time-zero variability.

- Complete methodology developed from test circuit layout to time-dependent variability-aware design.

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THE PRESENTER IS THANKFUL TO

- H. Reisinger, K. Rott,...
- A. Asenov, S. Amoroso, L. Gerrer, C. Millar, R. Hussin, F. Buchori...
- V. Afanas’ev, A. Stesmans, ...
- G. Gielen, S. Mahato, E. Maricau, P. De Wit, ...
- A. Kerber, T. Nigam, E. Cartier, E. Wu, J. Stathis ...
- J. Martin-Martinez, R. Fernandez, R. Rodriguez, M. Nafria...
- J. Zhang, Z. Ji, M. Duan, ...
- G. Wirth, V. V. de Almeida Camargo, M. B. da Silva, ...
- C. Chen, J. Watt, L. Li, K. Chanda,...
- V. Huard,...
- F. Crupi, L. Trojman, L. M. Procel,...
- A. Chaudhary, S. Mukhopadhyay, S. Mahapatra, A. Alam, ...
- P. Pfeifer, Z. Pliva, ...
- M. Karner, C. Kernstock, O. Baumgartner...
- K.-U. Giering, R. Jancke, D. Helms...
- A. Kuo, P. Tsang...